APPLICATION

FOR

UNITED STATES LETTERS PATENT

TITLE: ACTIVE PIXEL SENSOR WITH INTRA-PIXEL CHARGE TRANSFER

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CERTIFICATE OF MAILING BY EXPRESS MAIL

Express Mail Label No. EV399289283US

November 12, 2003

Date of Deposit

JPL Case No. C-19246 PATENT APPLICATION
CIT Case No. 2247
Attorney Docket No. JPL/096-93

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BACKGROUND OF THE INVENTION

Origin of the Invention:

The invention described herein was made in the performance of work under a NASA contract, and is subject to the provisions of Public Law 96-517 (35 USC 202) in which the Contractor has elected to retain title.

Technical Field:

The invention is related to semiconductor imaging devices and in particular to a silicon imaging device which can be fabricated using a standard CMOS process.

Background Art:

There are a number of types of semiconductor imagers, including charge coupled devices, photodiode arrays, charge injection devices and hybrid focal plane arrays. Charge coupled devices enjoy a number of advantages because they are an incumbent technology, they are capable of large formats and very small pixel size and they facilitate noiseless charge domain processing techniques (such as binning and time delay integration). However, charge coupled device imagers suffer from a number of disadvantages. For example, they exhibit destructive signal read-out and their signal fidelity decreases as the charge transfer efficiency raised to the power of the number of stages, so that they must have a nearly perfect charge transfer efficiency. They are particularly susceptible to radiation damage, they require good light shielding to avoid smear and they have high power dissipation for large arrays.

In order to ameliorate the charge transfer inefficiency problem, charge coupled device (CCD) imagers are fabricated with a specialized CCD semiconductor fabrication process to maximize their charge transfer efficiency. The difficulty is that the standard CCD process is incompatible with complementary metal oxide semiconductor (CMOS) processing, while the image signal processing electronics required for the imager are best fabricated in CMOS. Accordingly, it is impractical to integrate on-chip signal processing electronics in a CCD imager. Thus, the signal processing electronics is off-chip. Typically, each column of CCD pixels is transferred to a corresponding cell of a serial output register, whose output is amplified by a single on-chip amplifier (e.g., a source follower transistor) before being processed in off-chip signal processing electronics. As a result, the read-out frame rate is limited by the rate at which the on-chip amplifier can handle charge packets divided by the number of pixels in the imager.

The other types of imager devices have problems as well. Photodiode arrays exhibit high noise due to so-called kTC noise which makes it impossible to reset a diode or capacitor node to the same initial voltage at the beginning of each integration period. Photodiode arrays also suffer from lag. Charge injection devices also suffer from high noise, but enjoy the advantage of non-destructive readout over charge coupled devices.

Hybrid focal plane arrays exhibit less noise but are prohibitively expensive for many applications and have relatively small array sizes (e.g., 512-by-512 pixels).

What is needed is an imager device which has the low kTC noise level of a CCD without suffering from the destructive readout tendencies of a CCD.

SUMMARY OF THE DISCLOSURE

The invention is embodied in an imaging device formed as a monolithic complementary metal oxide semiconductor integrated circuit in an industry standard complementary metal oxide semiconductor process, the integrated circuit including a focal plane array of pixel cells, each one of the cells including a photogate overlying the substrate for accumulating photo-generated charge in an underlying portion of the substrate, a readout circuit including at least an output field effect transistor formed in the substrate, and a charge coupled device section formed on the substrate adjacent the photogate having a sensing node connected to the output transistor and at least one charge coupled device stage for transferring charge from the underlying portion of the substrate to the sensing node.

In a preferred embodiment, the sensing node of the charge coupled device stage includes a floating diffusion, and the charge coupled device stage includes a transfer gate overlying the substrate between the floating diffusion and the photogate. This preferred embodiment can further include apparatus for periodically resetting a potential of the sensing node to a predetermined potential, including a drain diffusion connected to a drain bias voltage and a reset gate between the floating diffusion and the drain diffusion, the reset gate connected to a reset control signal.

Preferably, the output transistor is a field effect source follower transistor, the floating diffusion being

connected to a gate of the source follower transistor. Preferably, the readout circuit further includes a double correlated sampling circuit having an input node connected to the output transistor. In the preferred implementation, the double correlated sampling circuit samples the floating diffusion immediately after it has been reset at one capacitor and then, later, at the end of the integration period at another capacitor. The difference between the two capacitors is the signal output. In accordance with a further refinement, this difference is corrected for fixed pattern noise by subtracting from it another difference sensed between the two capacitors while they are temporarily shorted.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a diagram illustrating the architecture of an individual focal plane cell of the invention.

FIG. 2 is a plan view of an integrated circuit constituting a focal plane array of cells of the type illustrated in FIG. 1.

FIG. 3 is a schematic diagram of the cell of FIG. 1.

FIG. 4 is a graph of the surface potential in the the charge transfer section of the cell of FIG. 3

FIG. 5 is a cross-sectional view of an alternative embodiment of the focal plane array of FIG. 2 including a micro-lens layer.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIG. 1 is a simplied block diagram of one pixel cell of a focal plane array of many such cells formed in an

integrated circuit. Each cell 10 includes a photogate 12, a charge transfer section 14 adjacent the photogate 12 and a readout circuit 16 adjacent the charge transfer section 14. FIG. 2 shows a focal plane array of many cells 10 formed on a silicon substrate 20. FIG. 3 is a simplified schematic diagram of a cell 10. Referring to FIG. 3, the photogate 12 consists of a relative large photogate electrode 30 overlying the substrate 20. The charge transfer section 14 consists of a transfer gate electrode 35 adjacent the photogate electrode 30, a floating diffusion 40, a reset electrode 45 and a drain diffusion 50. The readout circuit 16 consists of a source follower field effect transistor (FET) 55, a row select FET 60, a load FET 65 and a correlated double sampling circuit 70.

Referring to the surface potential diagram of FIG. 4, the photogate electrode 30 is held by a photogate signal PG at a positive voltage to form a potential well 80 in the substrate 20 in which photo-generated charge is accumulated during an integration period. The transfer gate electrode 35 is initially held at a less positive voltage by a transfer gate signal TX to form a potential barrier 85 adjacent the potential well 80. The floating diffusion 40 is connected to the gate of the source follower FET 55 whose drain is connected to a drain supply voltage VDD. The reset electrode 45 is initially held by a reset signal RST at a voltage corresponding to the voltage on the transfer gate 30 to form a potential barrier 90 thereunder. The drain supply voltage VDD connected to the drain diffusion 50 creates a constant potential well 95 underneath the drain diffusion 50.

During the integration period, electrons accumulate in the potential well 80 in proportion to photon flux incident

on the substrate 20 beneath the photogate electrode 30. At the end of the integration period, the surface potential beneath the floating diffusion 40 is quickly reset to a potential level 100 slightly above the potential well 95. This is accomplished by the reset signal RST temporarily increasing to a higher positive voltage to temporarily remove the potential barrier 90 and provide a downward potential staircase from the transfer gate potential barrier 85 to the drain diffusion potential well 95, as indicated in the drawing of FIG. 4. After the reset gate 45 is returned to its initial potential (restoring the potential barrier 90), the readout circuit 70 briefly samples the potential of the floating diffusion 40, and then the cell 10 is ready to transfer the photo-generated charge from beneath the photogate electrode 30. For this purpose, the photogate signal PG decreases to a less positive voltage to form a potential barrier 105 beneath the photogate electrode 30 and thereby provide a downward staircase surface potential from the photogate electrode 30 to the potential well 100 beneath the floating diffusion 40. This transfers all of the charge from beneath the photogate electrode 30 to the floating diffusion 40, changing the potential of the floating diffusion 40 from the level (100) at which it was previously reset to a new level 107 indicative of the amount of charge accumulated during the integration period. This new potential of the floating diffusion 40 is sensed at the source of the source follower FET 55. However, before the readout circuit 70 samples the source of the source follower FET 55, the photogate signal PG returns to its initial (more positive) voltage. The entire process is repeated for the next integration period.

The readout circuit 70 consists of a signal sample and hold (S/H) circuit including an S/H FET 200 and a signal

store capacitor 205 connected through the S/H FET 200 and through the row select FET 60 to the source of the source follower FET 55. The other side of the capacitor 205 is connected to a source bias voltage VSS. The one side of the capacitor 205 is also connected to the gate of an output FET 210. The drain of the output FET is a connected through a column select FET 220 to a signal sample output node VOUTS and through a load FET 215 to the drain voltage VDD. A signal called "signal sample and hold" (SHS) briefly turns on the S/H FET 200 after the charge accumulated beneath the photogate electrode 30 has been transferred to the floating diffusion 40, so that the capacitor 205 stores the source voltage of the source follower FET 55 indicating the amount of charge previously accumulated beneath the photogate electrode 30.

The readout circuit 70 also consists of a reset sample and hold (S/H) circuit including an S/H FET 225 and a signal store capacitor 230 connected through the S/H FET 225 and through the row select FET 60 to the source of the source follower FET 55. The other side of the capacitor 230 is connected to the source bias voltage VSS. The one side of the capacitor 230 is also connected to the gate of an output FET 240. The drain of the output FET 240 is connected through a column select FET 245 to a reset sample output node VOUTR and through a load FET 235 to the drain voltage VDD. A signal called "reset sample and hold" (SHR) briefly turns on the S/H FET 225 immediately after the reset signal RST has caused the resetting of the potential of the floating diffusion 40, so that the capacitor 230 stores the voltage at which the floating diffusion has been reset to.

The readout circuit provides correlated double sampling of the potential of the floating diffusion, in that the

charge integrated beneath the photogate 12 each integration period is obtained at the end of each integration period from the difference between the voltages at the output nodes VOUTS and VOUTR of the readout circuit 70. This eliminates the effects of kTC noise because the difference between VOUTS and VOUTR is independent of any variation in the reset voltage RST, a significant advantage.

Referring to FIG. 5, a transparent refractive microlens layer 110 may be deposited over the top of the focal plane array of FIG. 2. The microlens layer 110 consists of spherical portions 115 centered over each of the cells 10 and contoured so as to focus light toward the center of each photogate 12. This has the advantage of using light that would otherwise fall outside of the optically active region of the photogate 12. For example, at least some of the light ordinarily incident on either the charger transfer section 14 or the readout circuit 16 (FIG. 1) would be sensed in the photogate area with the addition of the microlens layer 110.

Preferably, the focal plane array corresponding to FIGS. 1-4 is implemented in CMOS silicon using an industry standard CMOS fabrication process. Preferably, each of the FETs is a MOSFET, the FETs 55, 60, 65, 200 and 225 being n-channel devices and the FETs 210, 220, 225, 230. 240, 245 being p-channel devices. The n-channel MOSFETS and the CCD channel underlying the gate electrodes 30, 35, 45 and the diffusions 40 and 50 may be located in a p-well while the remaining (p-channel) devices are located outside of the p-well. The gate voltage VLP applied to the gates of the p-channel load FETs 215 and 235 is a constant voltage on the order of +2.5 volts. The gate voltage VLN applied to the n-channel load FET 65 is a constant voltage on the order of

+1.5 volts.

Since the charge transfer section 14 involves only a single CCD stage between the photogate 12 and the floating diffusion 40 in the specific embodiment of FIG. 3, there is no loss due to charge transfer inefficiency and therefore there is no need to fabricate the device with a special CCD process. As a result, the readout circuit 70 as well as the output circuitry of the FETs 55, 60 and 65 can be readily implemented as standard CMOS circuits, making them extremely inexpensive. However, any suitable charge coupled device architecture may be employed to implement the charge transfer section 14, including a CCD having more than one stage. For example, two or three stages may be useful for buffering two or three integration periods.

Other implementations of the concept of the invention may be readily constructed by the skilled worker in light of the foregoing disclosure. For example, the floating diffusion 40 may instead be a floating gate electrode. The signal and reset sample and hold circuits of the readout circuit 70 may be any suitable sample and hold circuits. Moreover, shielding of the type well-known in the art may be employed defining an aperture surrounding the photogate 12. Also, the invention may be implemented as a buried channel device.

Another feature of the invention which is useful for eliminating fixed pattern noise due to variations in FET threshold voltage across the substrate 20 is a shorting FET 116 across the sampling capacitors 205, 235. After the accumulated charge has been measured as the potential difference between the two output nodes VOUTS and VOUTR, a shorting signal VM is temporarily applied to the gate of the

shorting FET 116 and the VOUTS-to-VOUTR difference is measured again. This latter difference is a measure of the disparity between the threshold voltages of the output FETs 210, 240, and may be referred to as the fixed pattern difference. The fixed pattern difference is subtracted from the difference between VOUTS and VOUTR measured at the end of the integration period, to remove fixed pattern noise.

As previously mentioned herein, a floating gate may be employed instead of the floating diffusion 40. Such a floating gate is indicated schematically in FIG. 3 by a simplified dashed line floating gate electrode 41.

Preferably, the invention is fabricated using an industry standard CMOS process, so that all of the dopant concentrations of the n-channel and p-channel devices and of the various diffusions are in accordance with such a process. In one implementation, the area of the L-shaped photogate 12 (i.e., the photogate electrode 30) was about 100 square microns; the transfer gate electrode 35 and the reset gate electrode were each about 1.5 microns by about 6 microns; the photogate signal PG was varied between about +5 volts (its more positive voltage) and about 0 volts (its less positive voltage; the transfer gate signal TX was about +2.5 volts; the reset signal RST was varied between about +5 volts (its more positive voltage) and about +2.5 volts (its less positive voltage); the drain diffusion 50 was held at about +5 volts.

While the invention has been described in detail by specific reference to preferred embodiments, it is understood that variations and modifications may be made without departing from the true spirit and scope of the invention.